

**Features:**

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM}, V_{RSM}	V_{DRM}, V_{RRM}	Type & Outline
2100V	2000V	MTx350-20-415F3
2300V	2200V	MTx350-22-415F3
2600V	2500V	MTx350-25-415F3

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^{\circ}\text{C})$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c=85^{\circ}\text{C}$	125			350	A
$I_{T(RMS)}$	RMS on-state current					549	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			40	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			10	kA
I^2t	I^2t for fusing coordination	$V_R=60\%V_{RRM}$				500	$\text{A}^2\text{s}\cdot 10^3$
V_{TO}	Threshold voltage		125			0.84	V
r_T	On-state slope resistance					0.50	m Ω
V_{TM}	Peak on-state voltage	$I_{TM}=1050\text{A}$	25			1.89	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=67\%V_{DRM}$	125			800	V/ μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A $t_i \leq 0.5\mu\text{s}$ Repetitive	125			100	A/ μs
I_{GT}	Gate trigger current	$V_A=12\text{V}$, $I_A=1\text{A}$	25	30		200	mA
V_{GT}	Gate trigger voltage			0.7		2.5	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.09	$^{\circ}\text{C}/\text{W}$
$R_{th(c-h)}$	Thermal resistance case to heat sink	Single side cooled per chip				0.04	$^{\circ}\text{C}/\text{W}$
V_{iso}	Isolation voltage	50Hz, R.M.S, $t=1\text{min}$, $I_{iso}:1\text{mA}(\text{MAX})$		3000			V
F_m	Terminal connection torque (M10)				12.0		N·m
	Mounting torque (M6)				6.0		N·m
T_{vj}	Junction temperature			-40		125	$^{\circ}\text{C}$
T_{stg}	Stored temperature			-40		125	$^{\circ}\text{C}$
W_t	Weight				1275		g
Outline	415F3						

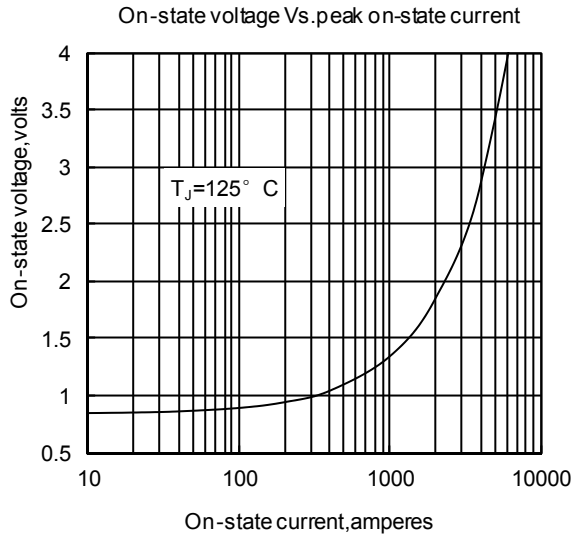


Fig. 1

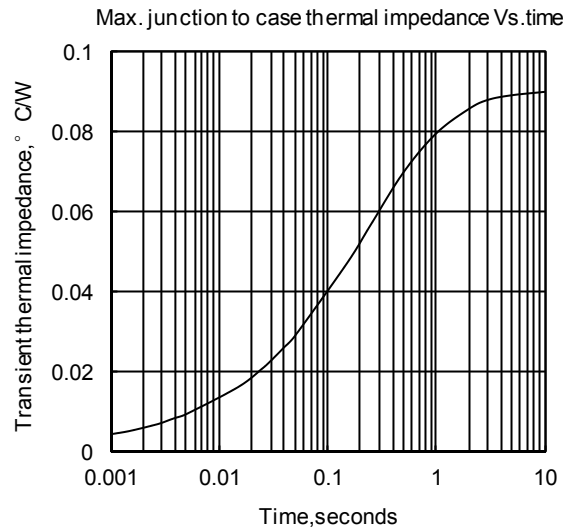


Fig. 2

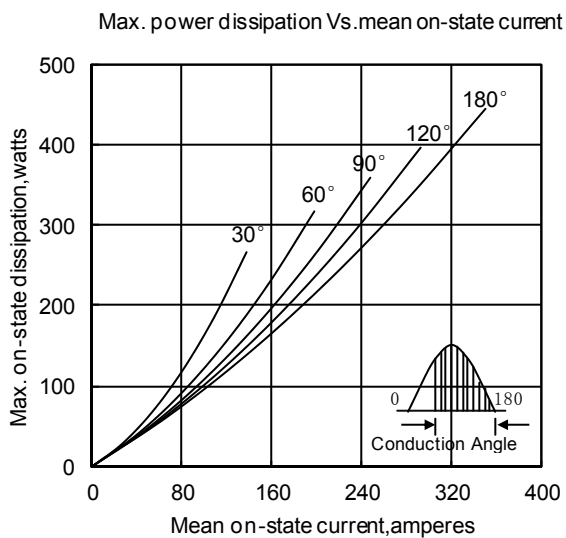


Fig. 3

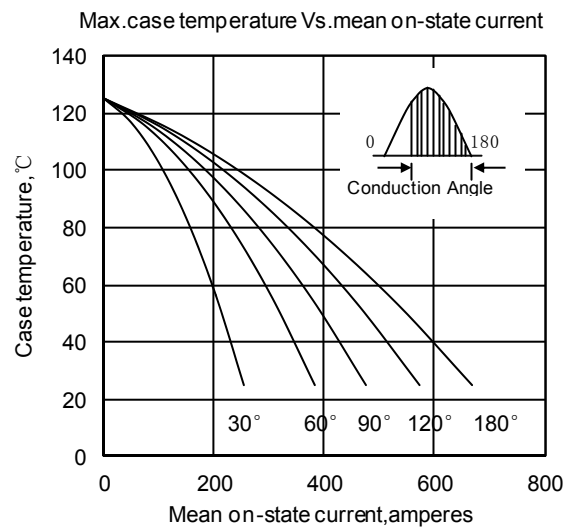


Fig. 4

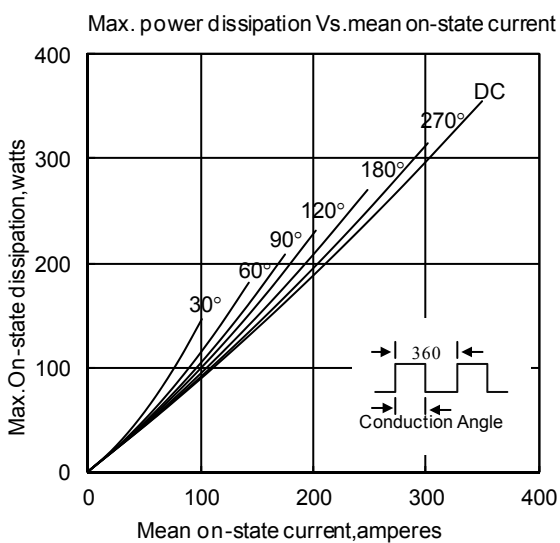


Fig. 5

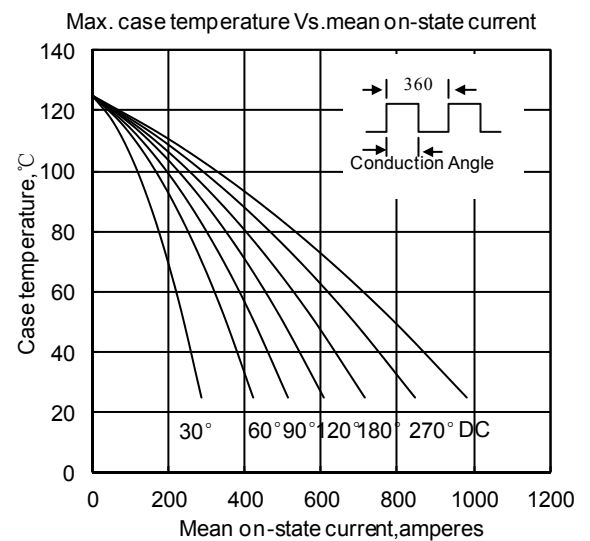


Fig. 6

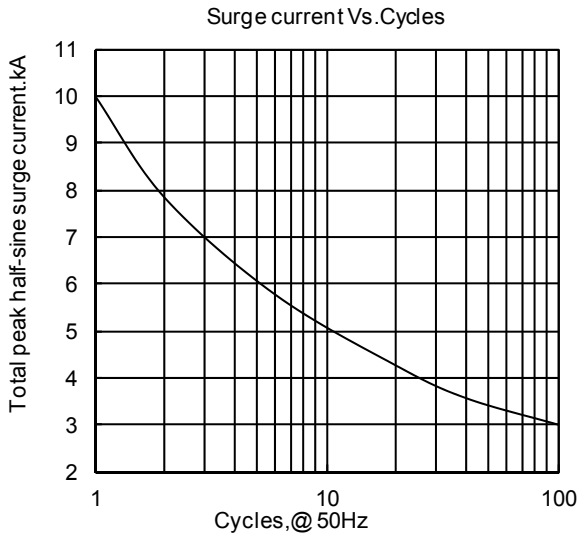


Fig. 7

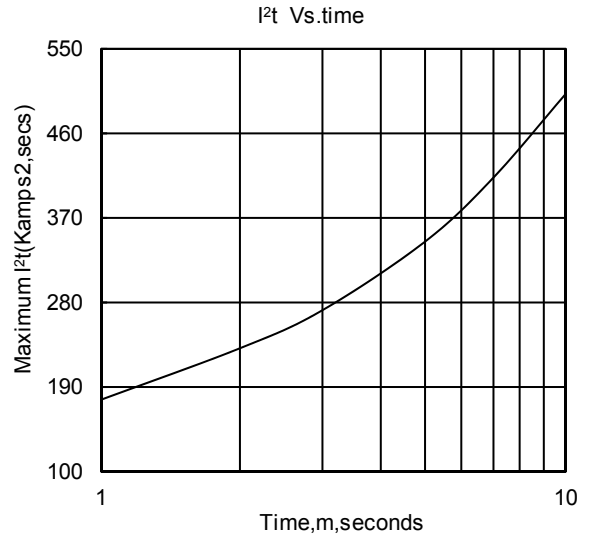


Fig. 8

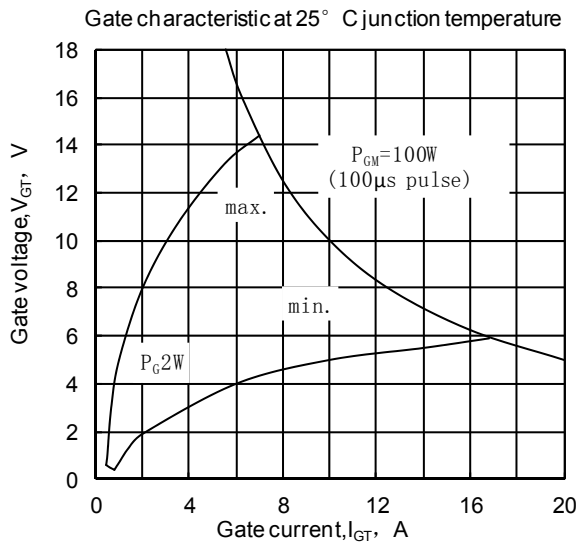


Fig. 9

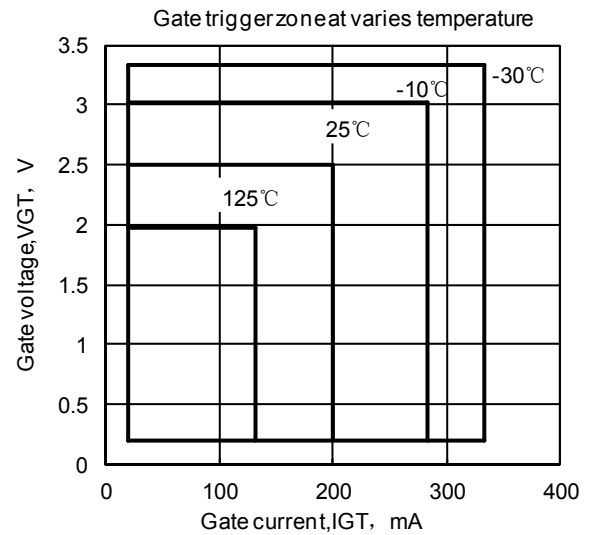


Fig. 10

Outline:

