Features：

- Isolated mounting base 2500V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM},V_{RSM}	V_{DRM},V_{RRM}	Type & Outline
900V	800V	MFx182-08-216F3/216F3B
1100V	1000V	MFx182-10-216F3/216F3B
1300V	1200V	MFx182-12-216F3/216F3B
1500V	1400V	MFx182-14-216F3/216F3B
1700V	1600V	MFx182-16-216F3/216F3B
1900V	1800V	MFx182-18-216F3/216F3B

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled,T_c=85°C	125			182	A
$I_{T(RMS)}$	RMS on-state current					286	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			20	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	125			7	kA
I^2t	I^2t for fusing coordination					245	A^2s*10^3
V_{TO}	Threshold voltage		125			0.80	V
r_T	On-state slope resistance					1.26	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=550A	25			1.62	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t_r ≤0.5μs Repetitive	125			100	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		150	mA
V_{GT}	Gate trigger voltage			0.7		2.5	V
I_H	Holding current			10		150	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.16	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.08	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I_{iso}:1mA(MAX)		2500			V
F_m	Terminal connection torque(M6)				6.0		N·m
	Mounting torque(M6)				6.0		N·m
T_{vj}	Junction temperature			-40		125	°C
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				320		g
Outline	216F3、216F3B						

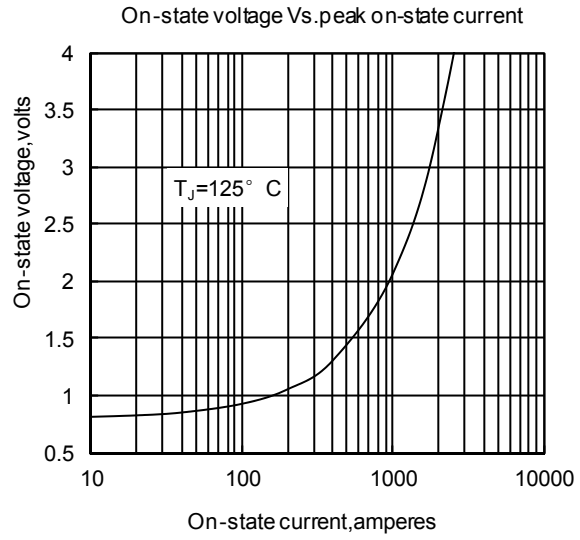


Fig1

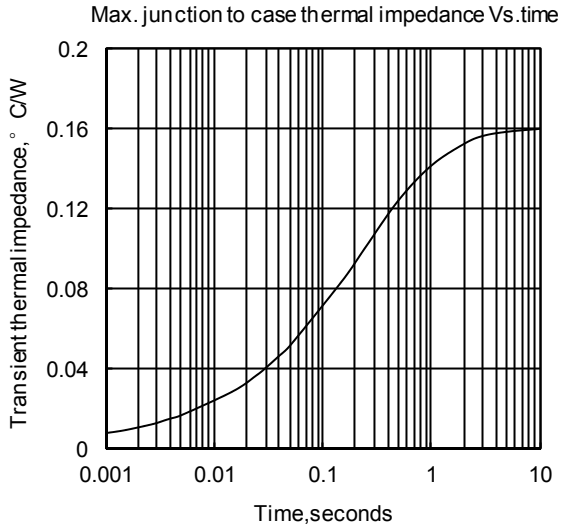


Fig2

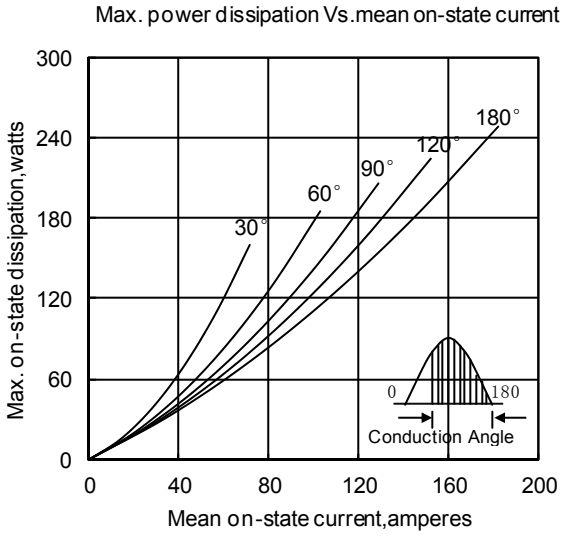


Fig3

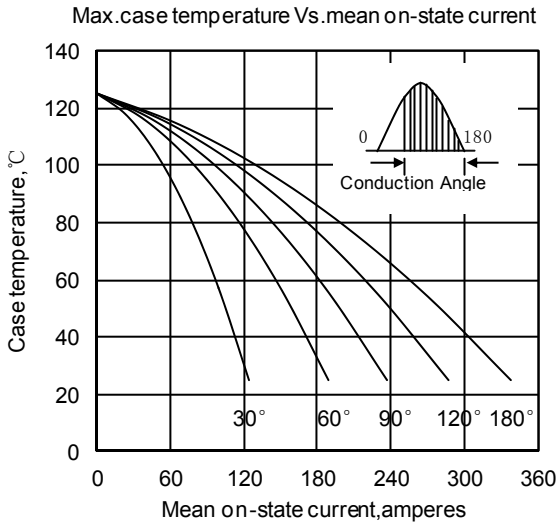


Fig4

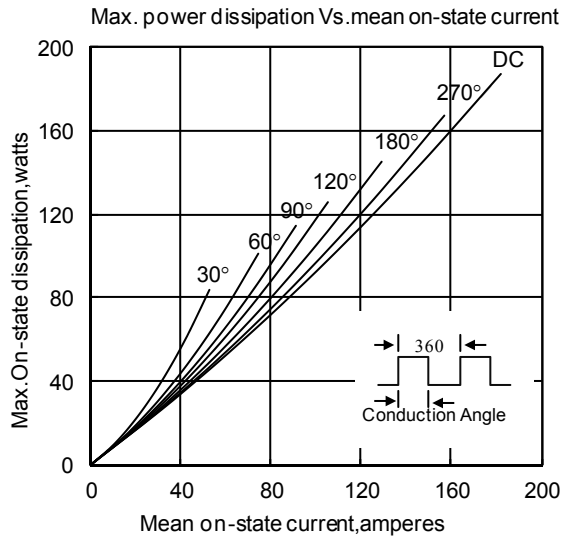


Fig5

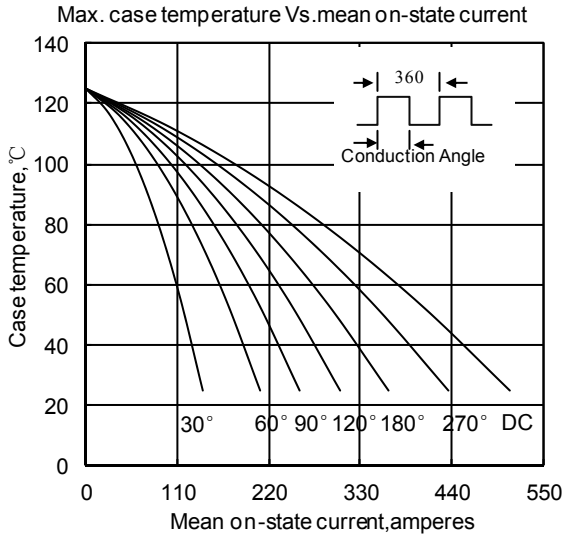


Fig6

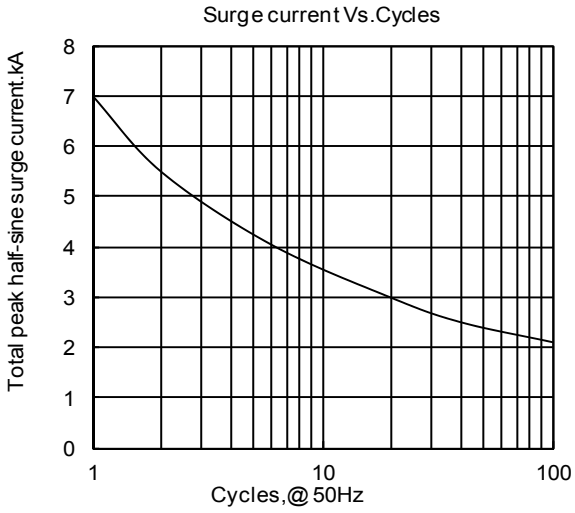


Fig7

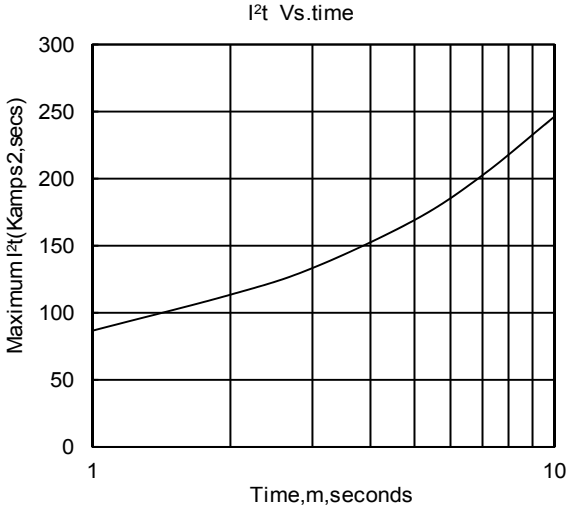


Fig8

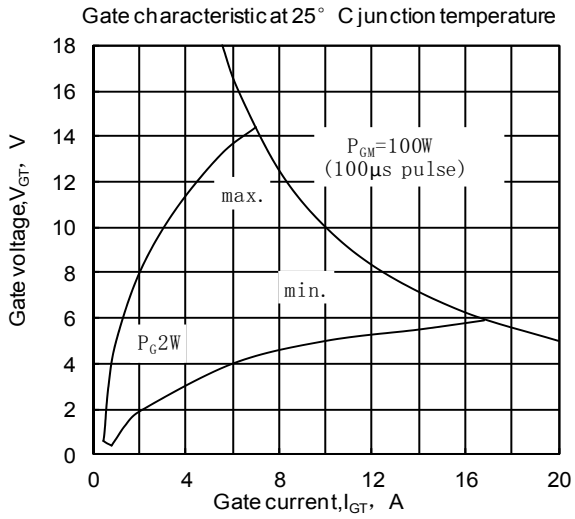


Fig9

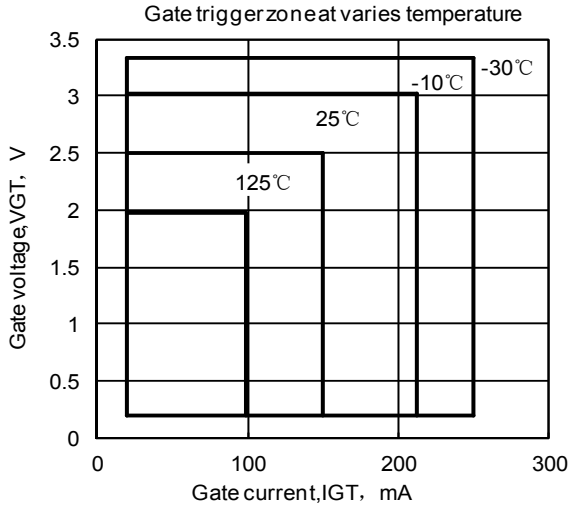
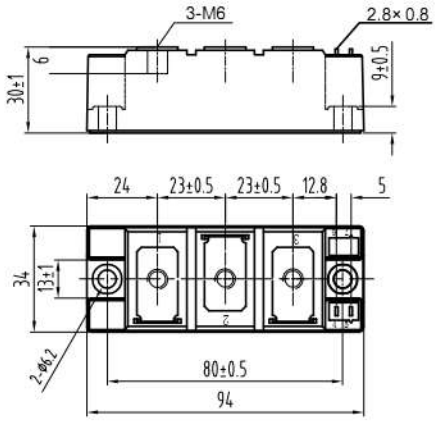
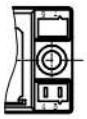


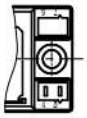
Fig10

Outline:





216F3: 4 is Gate



216F3B: 5 is Gate